SN74LVC1G19 1-of-2 Decoder and Demultiplexer

1 Features

- Available in the Texas Instruments NanoFree™ Package
- Supports 5-V V_{CC} Operation
- Inputs Accept Voltages to 5.5 V
- Supports Down Translation to V_{CC}
- Maximum t_{pd} of 4 ns at 3.3 V
- Low Power Consumption, 10-µA Maximum I_{CC}
- ±24-mA Output Drive at 3.3 V
- V_{OLP} (Output Ground Bounce) <0.8 V Typical at V_{CC} = 3.3 V, T_A = 25°C
- V_{OHV} (Output V_{OH} Undershoot) >2 V Typical at V_{CC} = 3.3 V, T_A = 25°C
- I_{off} Supports Live Insertion, Partial-Power-Down Mode, and Back-Drive Protection
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

2 Applications

- AV Receivers
- Audio Docks: Portable
- Blu-ray® Players and Home Theater
- MP3 Players/Recorders
- Personal Digital Assistants (PDAs)
- Power: Telecom/Server AC/DC Supply: Single Controller: Analog and Digital
- Solid State Drives (SSDs): Client and Enterprise
- TVs: LCD/Digital and High-Definition (HDTVs)
- Tablets: Enterprise
- Video Analytics: Server
- Wireless Headsets, Keyboards, and Mice

3 Description

This decoder/demultiplexer is designed for 1.65-V to 5.5-V V_{CC} operation.

The SN74LVC1G19 device is a 1-of-2 decoder / demultiplexer. When $\overline{E}$ input is high, the decoder will be disabled and both outputs will be high. When $\overline{E}$ input is low, the A input selects which output will be low.

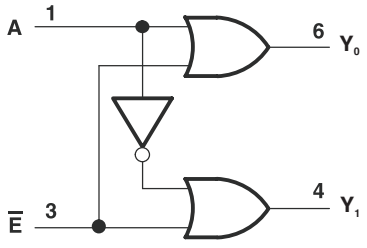
This device is fully specified for partial-power-down applications using I_{off}.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74LVC1G19DBV	SOT-23 (6)	2.9 mm × 1.6 mm
SN74LVC1G19DCK	SC70 (6)	2.0 mm × 1.25 mm
SN74LVC1G19DRL	SOT (6)	1.6 mm × 1.2 mm
SN74LVC1G19DRY	SON (6)	1.45 mm × 1.0 mm
SN74LVC1G19YZP	DSBGA (6)	1.41 mm × 0.91 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

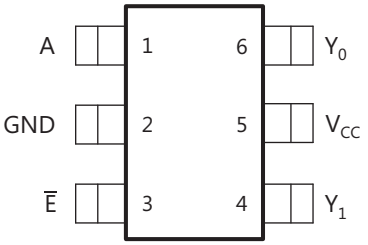
Changes from Revision F (July 2012) to Revision G **Page**

- Added *Applications* section, *Device Information* table, *Pin Configuration and Functions* section, *ESD Ratings* table, *Thermal Information* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Deleted *Ordering Information* table. ... 1
- Updated I_{off} in *Features*. ... 1

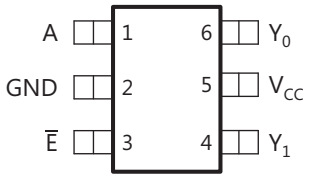
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5 Pin Configuration and Functions

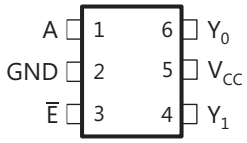
DBV Package
6-Pin SOT-23
Top View



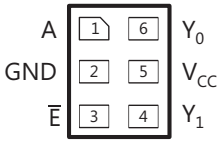
DCK Package
6-Pin SC70
Top View



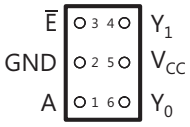
DRL Package
6-Pin SOT
Top View



DRY Package
6-Pin SON
Top View



YZP Package
6-Pin DSBGA
Bottom View



Pin Functions[1]

PIN		I/O	DESCRIPTION
NAME	NO.		
A	1	I	Adress input, selects which output goes low.
GND	2	—	Ground
$\overline{E}$	3	I	Enable input, active low
Y_1	4	O	Output 1, low when selected by A high and $\overline{E}$ low
V_{CC}	5	—	Power pin
Y_0	6	O	Output 0, low when selected by A low and $\overline{E}$ low

(1) See mechanical drawings for dimensions

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	6.5	V
V_I	Input voltage(2)		–0.5	6.5	V
V_O	Voltage applied to any output in the high-impedance or power-off state(2)		–0.5	6.5	V
V_O	Voltage applied to any output in the high or low state(2)(3)		–0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	V_I < 0		–50	mA
I_{OK}	Output clamp current	V_O < 0		–50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CC} or GND			±100	mA
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The value of V_{CC} is provided in the *Recommended Operating Conditions* table.

6.2 ESD Ratings

			VALUE	UNIT
V_{ESD}	Electrostatic discharge	Human Body Model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged-Device Model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1000	
		Machine model	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

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6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage	Operating	1.65	5.5	V
		Data retention only	1.5		
V_{IH}	High-level input voltage	V_{CC} = 1.65 V to 1.95 V	0.65 × V_{CC}		V
		V_{CC} = 2.3 V to 2.7 V	1.7		
		V_{CC} = 3 V to 3.6 V	2		
		V_{CC} = 4.5 V to 5.5 V	0.7 × V_{CC}		
V_{IL}	Low-level input voltage	V_{CC} = 1.65 V to 1.95 V		0.35 × V_{CC}	V
		V_{CC} = 2.3 V to 2.7 V		0.7	
		V_{CC} = 3 V to 3.6 V		0.8	
		V_{CC} = 4.5 V to 5.5 V		0.3 × V_{CC}	
V_I	Input voltage		0	5.5	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 1.65 V		–4	mA
		V_{CC} = 2.3 V		–8	
		V_{CC} = 3 V		–16	
				–24	
		V_{CC} = 4.5 V		–32	
I_{OL}	Low-level output current	V_{CC} = 1.65 V		4	mA
		V_{CC} = 2.3 V		8	
		V_{CC} = 3 V		16	
				24	
		V_{CC} = 4.5 V		32	
Δt/Δv	Input transition rise or fall rate	V_{CC} = 1.8 V ± 0.15 V, 2.5 V ± 0.2 V		20	ns/V
		V_{CC} = 3.3 V ± 0.3 V		10	
		V_{CC} = 5 V ± 0.5 V		5	
T_A	Operating free-air temperature		–40	85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, SCBA004.

6.4 Thermal Information

THERMAL METRIC(1)		SN74LVC1G19					UNIT
		DBV (SOT-23)	DCK (SC70)	DRL (SOT)	DRY (SON)	YZP (DSBGA)	
		6 PINS	6 PINS	6 PINS	6 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	165	259	142	234	123	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

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6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	MIN	TYP(1)	MAX	UNIT
V_{OH}	I_{OH} = –100 µA	1.65 V to 5.5 V	V_{CC} – 0.1			V
	I_{OH} = –4 mA	1.65 V	1.2			
	I_{OH} = –8 mA	2.3 V	1.9			
	I_{OH} = –16 mA	3 V	2.4			
	I_{OH} = –24 mA		2.3			
	I_{OH} = –32 mA	4.5 V	3.8			
V_{OL}	I_{OL} = 100 µA	1.65 V to 5.5 V			0.1	V
	I_{OL} = 4 mA	1.65 V			0.45	
	I_{OL} = 8 mA	2.3 V			0.3	
	I_{OL} = 16 mA	3 V			0.4	
	I_{OL} = 24 mA				0.55	
	I_{OL} = 32 mA	4.5 V			0.55	
I_I	V_I = 5.5 V or GND	0 to 5.5 V			±1	µA
I_{off}	V_I or V_O = 5.5 V	0			±10	µA
I_{CC}	V_I = 5.5 V or GND, I_O = 0	1.65 V to 5.5 V			10	µA
ΔI_{CC}	One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND	3 V to 5.5 V			500	µA
C_I	V_I = V_{CC} or GND	3.3 V		3.5		pF

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

6.6 Switching Characteristics, C_L = 15 pF

over recommended operating free-air temperature range, C_L = 15 pF (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 1.8 V ± 0.15 V		V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or $\overline{E}$	Y	2.5	16.1	1.5	5.9	1	4	0.5	2.8	ns

6.7 Switching Characteristics, C_L = 30 pF or 50 pF

over recommended operating free-air temperature range, C_L = 30 pF or 50 pF (unless otherwise noted) (see Figure 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 1.8 V ± 0.15 V		V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or $\overline{E}$	Y	3.2	16.1	1.5	6.5	1.1	5.2	0.5	3.9	ns

6.8 Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CC} = 1.8 V	V_{CC} = 2.5 V	V_{CC} = 3.3 V	V_{CC} = 5 V	UNIT
			TYP	TYP	TYP	TYP	
C_{pd}	Power dissipation capacitance	f = 10 MHz	15.5	16	16	18	pF

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6.9 Typical Characteristics

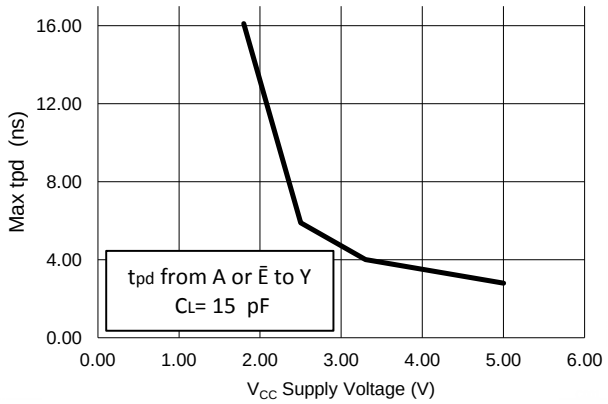


Figure 1. Time Propagation Delay vs V_{CC}, C_L= 15 pF

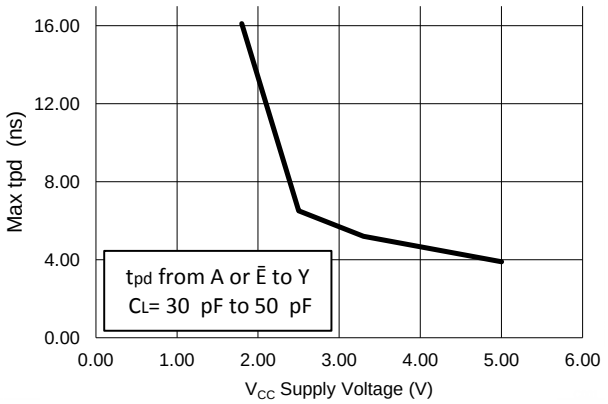
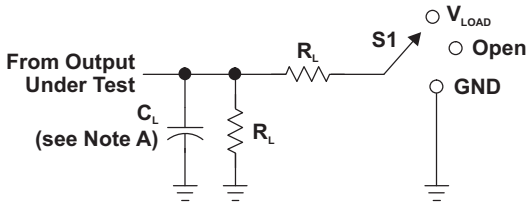


Figure 2. Time Propagation Delay vs V_{CC}, C_L= 30 pF or 50 pF

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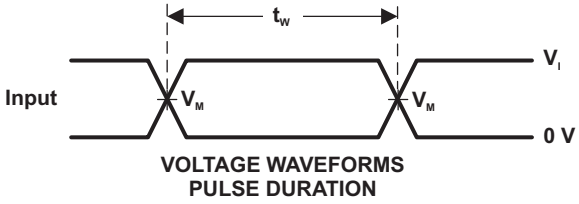
7 Parameter Measurement Information



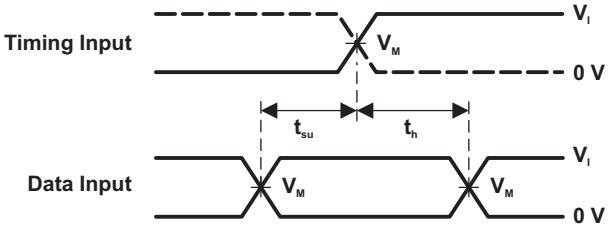
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

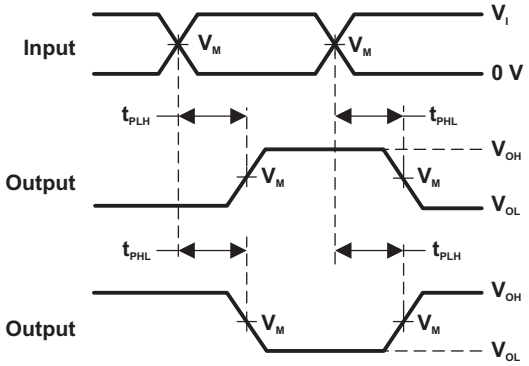
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.8 V ± 0.15 V	V_{CC}	≤2 ns	$V_{CC}/2$	2 × V_{CC}	15 pF	1 MΩ	0.15 V
2.5 V ± 0.2 V	V_{CC}	≤2 ns	$V_{CC}/2$	2 × V_{CC}	15 pF	1 MΩ	0.15 V
3.3 V ± 0.3 V	3 V	≤2.5 ns	1.5 V	6 V	15 pF	1 MΩ	0.3 V
5 V ± 0.5 V	V_{CC}	≤2.5 ns	$V_{CC}/2$	2 × V_{CC}	15 pF	1 MΩ	0.3 V



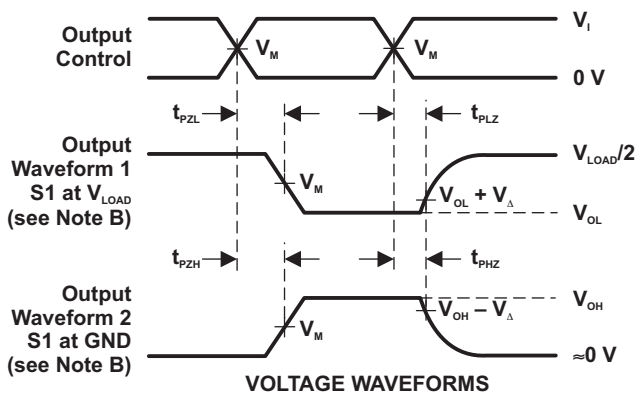
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



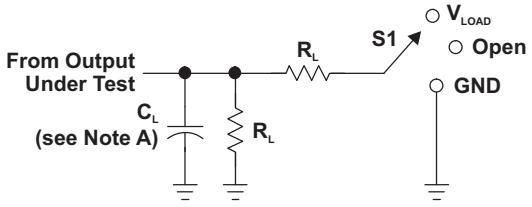
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuit and Voltage Waveforms

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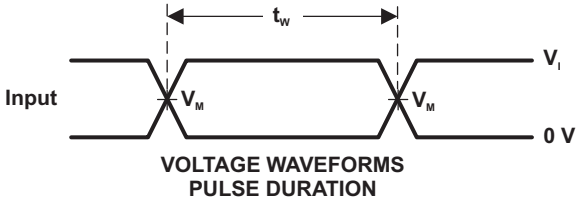
Parameter Measurement Information (continued)



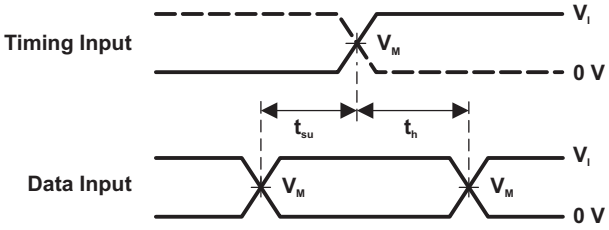
LOAD CIRCUIT

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t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

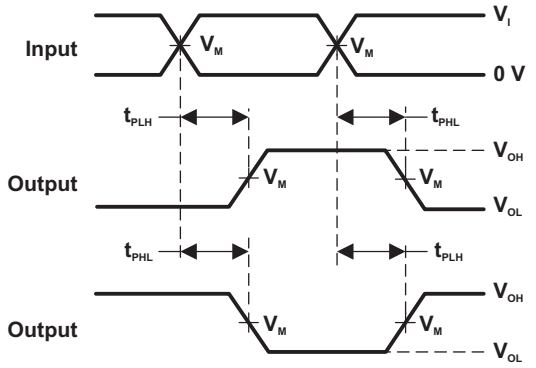
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.8 V ± 0.15 V	V_{CC}	≤2 ns	$V_{CC}/2$	2 × V_{CC}	30 pF	1 kΩ	0.15 V
2.5 V ± 0.2 V	V_{CC}	≤2 ns	$V_{CC}/2$	2 × V_{CC}	30 pF	500 Ω	0.15 V
3.3 V ± 0.3 V	3 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
5 V ± 0.5 V	V_{CC}	≤2.5 ns	$V_{CC}/2$	2 × V_{CC}	50 pF	500 Ω	0.3 V



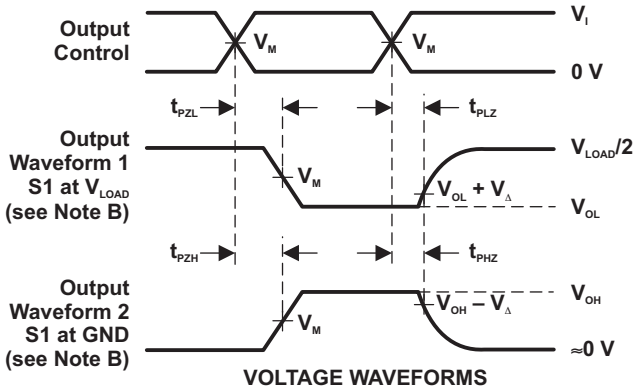
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
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C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω.
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E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

Figure 4. Load Circuit and Voltage Waveforms

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8 Detailed Description

8.1 Overview

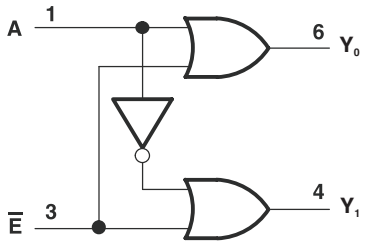
This decoder/demultiplexer is designed for 1.65-V to 5.5-V V_{CC} operation.

The SN74LVC1G19 device is a 1-of-2 decoder/demultiplexer. This device decodes the 1-bit address on input A and places a logic low on the matching address output, Y_0 or Y_1 , when the enable ($\overline{E}$) input signal is low.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

NanoFree package technology is a major breakthrough in IC packaging concepts, using the die as the package.

8.2 Functional Block Diagram



8.3 Feature Description

SN74LVC1G19 is available in NanoFree package. NanoFree is a major breakthrough in IC packaging concepts, it is a bare die package developed for applications that require the smallest possible package. The device supports 5-V V_{CC} Operation. All Inputs accept voltages up to 5.5 V. ±24-mA output drive at 3.3 V. The maximum time propagation delay (t_{pd}) is 5.4 ns at 3.3 V. Low Power Consumption, 10-µA Max I_{CC}. Typical output ground bounce (V_{OLP}) and Output V_{OH} Undershoot (V_{OHV}). This device is fully specified for partial-power-down applications using I_{off}. The I_{off} feature ensures that damaging current will not backflow through the device when it is powered down. The SN74LVC1G19 device has isolation during power off. I_{off} supports live insertion, partial-power-down mode and back drive protection.

8.4 Device Functional Modes

Table 1 lists the functional modes of the SN74LVC1G19.

Table 1. Function Table

INPUTS		OUTPUTS	
$\overline{E}$	A	Y_0	Y_1
L	L	L	H
L	H	H	L
H	X	H	H

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The SN74LVC1G19 device is a 1-of-2 decoder/demultiplexer. This device decodes the 1 bit address on input A and places a logic low on the matching address output, Y_0 or Y_1 , when the enable ($\overline{E}$) input signal is low. It can produce 24 mA of drive current at 3.3 V making it ideal for driving multiple outputs.

9.2 Typical Application

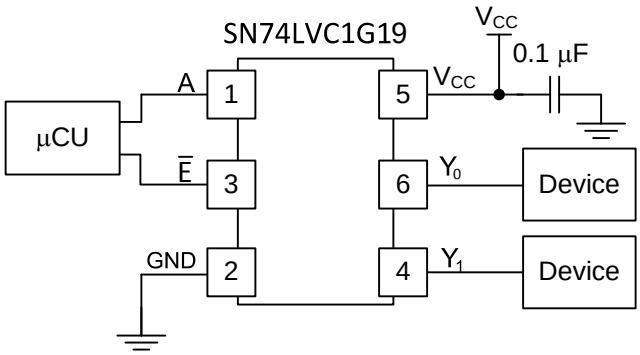


Figure 5. Typical Application Diagram

9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. Outputs can be combined to produce higher drive but the high drive will also create faster edges into light loads so routing and load conditions should be considered to prevent ringing.

9.2.2 Detailed Design Procedure

1. Recommended Input Conditions:
   - For rise time and fall time specifications, see ($\Delta t/\Delta V$) in *Recommended Operating Conditions* table.
   - For specified high and low levels, see (V_{IH} and V_{IL}) in *Recommended Operating Conditions* table.
   - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid V_{CC}.
2. Recommend Output Conditions:
   - Load currents must not exceed 50 mA per output and 100 mA total for the part.
   - Series resistors on the output may be used if the user desires to slow the output edge signal or limit the output current.

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Typical Application (continued)

9.2.3 Application Curve

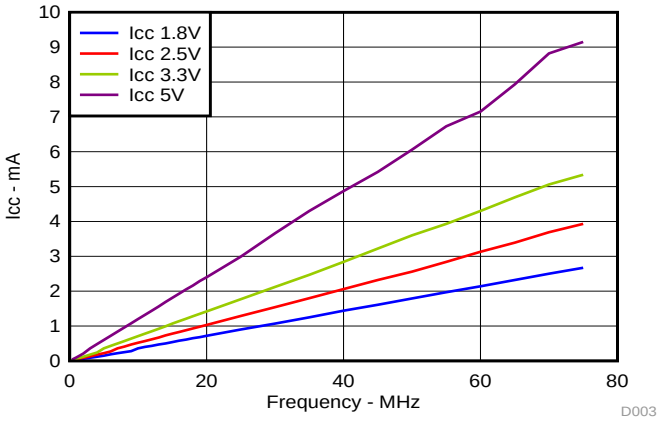


Figure 6. I_{CC} vs Frequency

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in *Absolute Maximum Ratings* table.

Each V_{CC} terminal must have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1-µF capacitor is recommended. If there are multiple V_{CC} terminals then 0.01-µF or 0.022-µF capacitors are recommended for each power terminal. It is ok to parallel multiple bypass capacitors to reject different frequencies of noise. Multiple bypass capacitors may be paralleled to reject different frequencies of noise. The bypass capacitor must be installed as close to the power terminal as possible for the best results.

11 Layout

11.1 Layout Guidelines

When using multiple bit logic devices, inputs must not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in Figure 7 are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC}, whichever makes more sense or is more convenient.

11.2 Layout Example

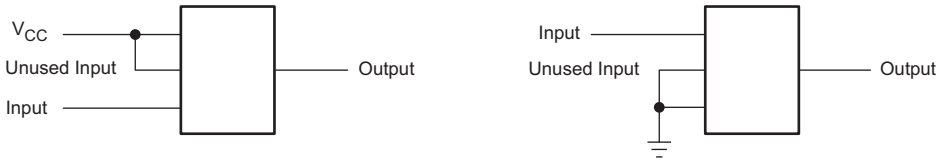


Figure 7. Layout Diagram

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12 Device and Documentation Support

12.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.2 Trademarks

NanoFree, E2E are trademarks of Texas Instruments.
Blu-ray is a registered trademark of Blu-ray Disc Association.
All other trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LVC1G19DBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(C195 ~ C19K ~ C19R)	Samples
SN74LVC1G19DBVRE4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(C195 ~ C19K ~ C19R)	Samples
SN74LVC1G19DBVRG4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(C195 ~ C19K ~ C19R)	Samples
SN74LVC1G19DBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(C195 ~ C19K ~ C19R)	Samples
SN74LVC1G19DCKR	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(CY5 ~ CYF ~ CYK ~ CYR)	Samples
SN74LVC1G19DCKRE4	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(CY5 ~ CYF ~ CYK ~ CYR)	Samples
SN74LVC1G19DCKRG4	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(CY5 ~ CYF ~ CYK ~ CYR)	Samples
SN74LVC1G19DRLR	ACTIVE	SOT	DRL	6	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(CY7 ~ CYR)	Samples
SN74LVC1G19DRLRG4	ACTIVE	SOT	DRL	6	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(CY7 ~ CYR)	Samples
SN74LVC1G19DRYR	ACTIVE	SON	DRY	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CY	Samples
SN74LVC1G19YZPR	ACTIVE	DSBGA	YZP	6	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	(CY7 ~ CYN)	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

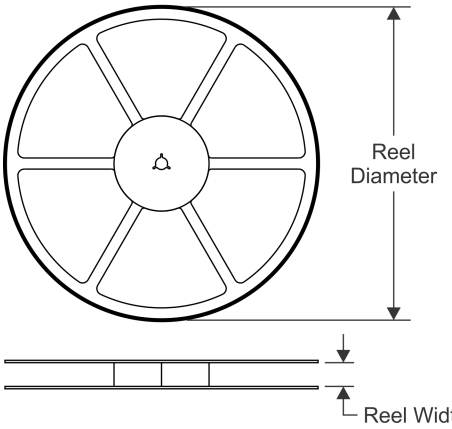
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

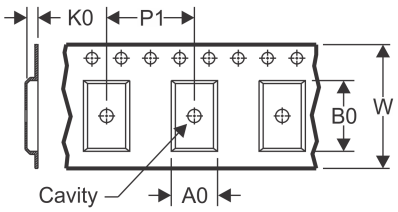
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

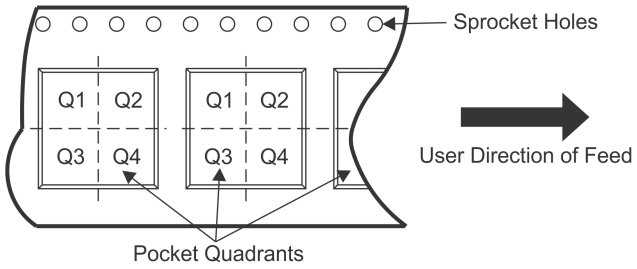


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

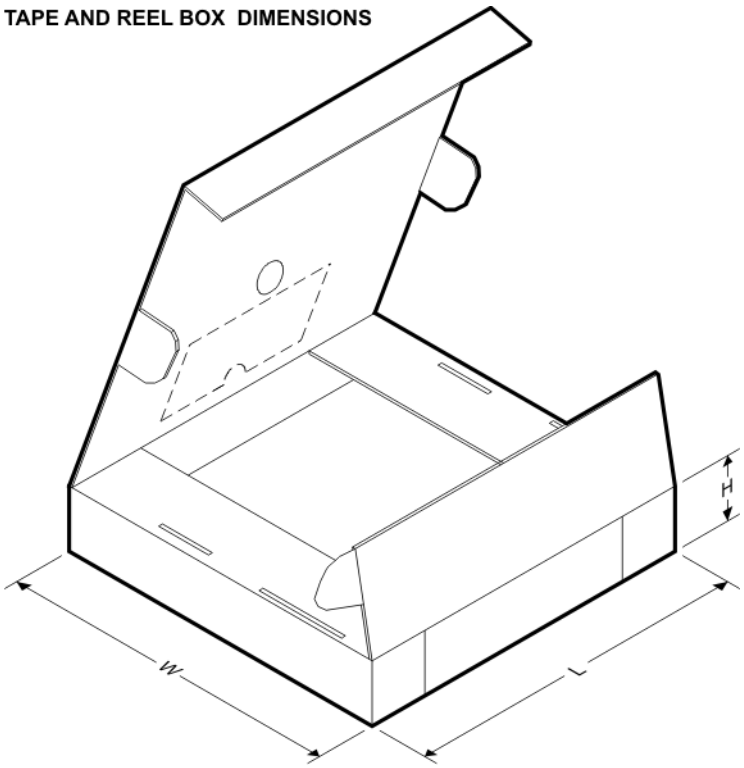
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC1G19DBVT	SOT-23	DBV	6	250	180.0	9.2	3.17	3.23	1.37	4.0	8.0	Q3
SN74LVC1G19DCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1G19DCKR	SC70	DCK	6	3000	180.0	9.2	2.3	2.55	1.2	4.0	8.0	Q3
SN74LVC1G19DCKR	SC70	DCK	6	3000	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74LVC1G19DRLR	SOT	DRL	6	4000	180.0	9.5	1.78	1.78	0.69	4.0	8.0	Q3
SN74LVC1G19DRLR	SOT	DRL	6	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
SN74LVC1G19DRYR	SON	DRY	6	5000	180.0	9.5	1.15	1.6	0.75	4.0	8.0	Q1
SN74LVC1G19YZPR	DSBGA	YZP	6	3000	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1

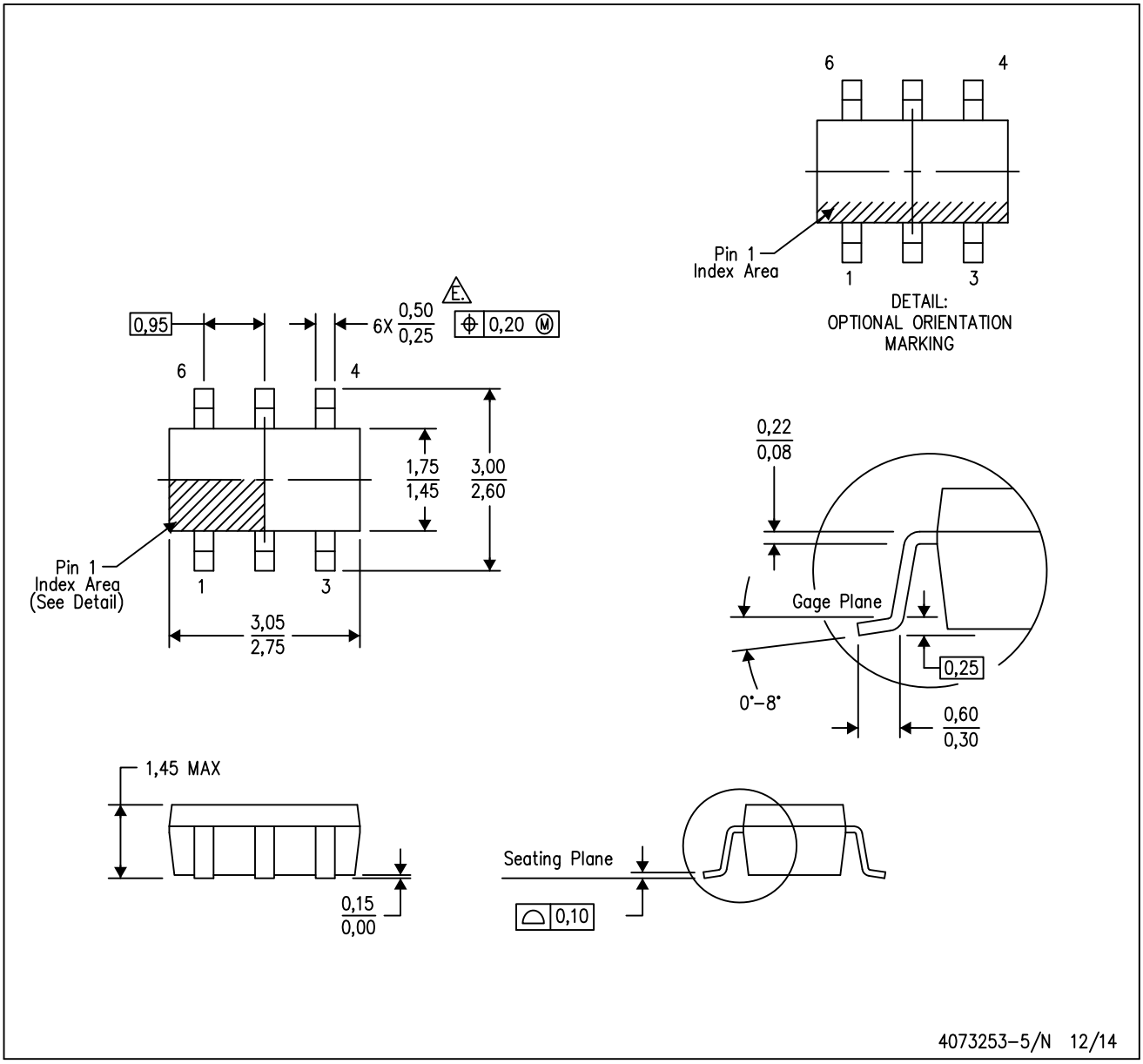
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

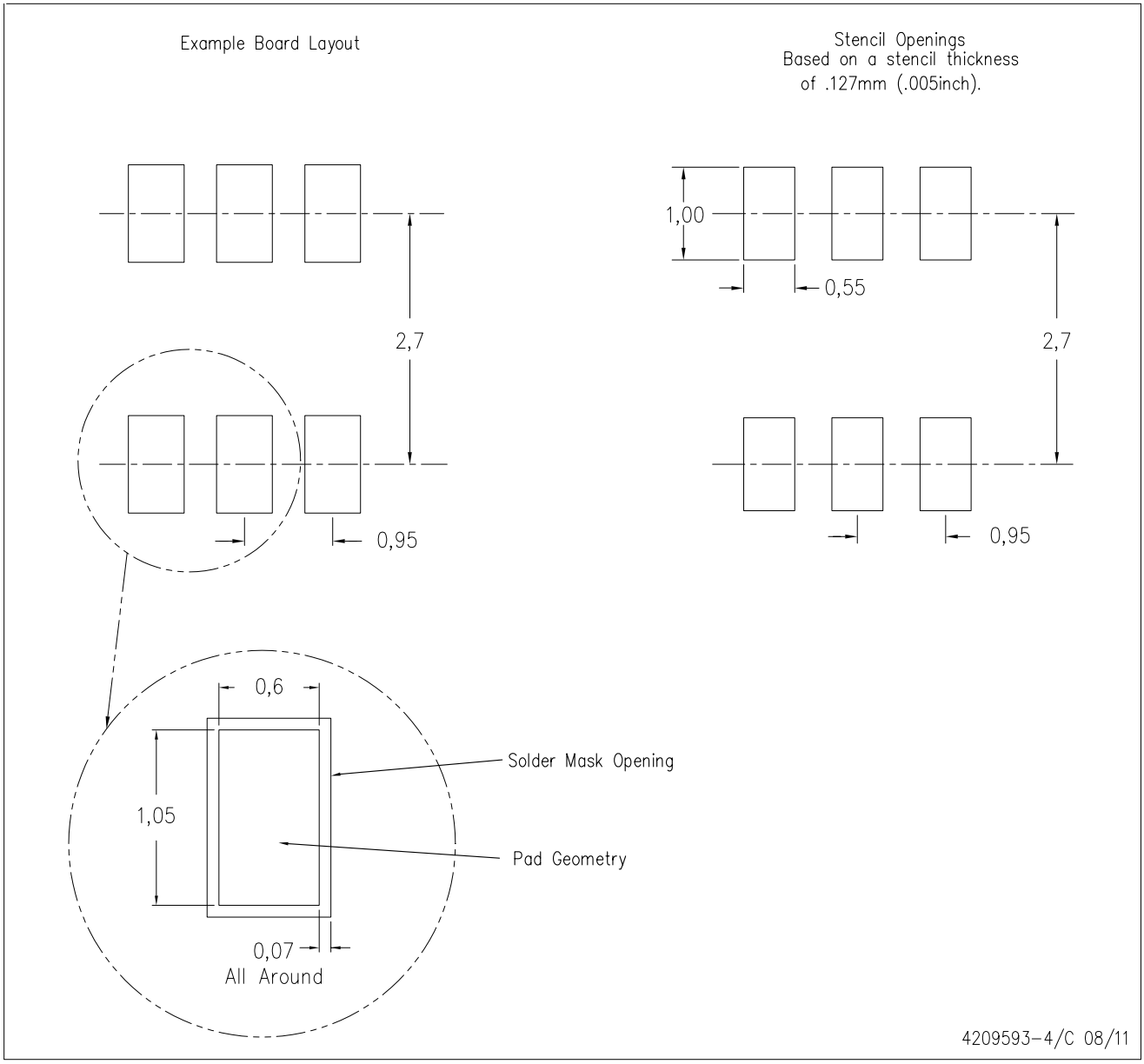
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC1G19DBVT	SOT-23	DBV	6	250	205.0	200.0	33.0
SN74LVC1G19DCKR	SC70	DCK	6	3000	180.0	180.0	18.0
SN74LVC1G19DCKR	SC70	DCK	6	3000	205.0	200.0	33.0
SN74LVC1G19DCKR	SC70	DCK	6	3000	180.0	180.0	18.0
SN74LVC1G19DRLR	SOT	DRL	6	4000	184.0	184.0	19.0
SN74LVC1G19DRLR	SOT	DRL	6	4000	202.0	201.0	28.0
SN74LVC1G19DRYR	SON	DRY	6	5000	184.0	184.0	19.0
SN74LVC1G19YZPR	DSBGA	YZP	6	3000	220.0	220.0	35.0

DBV (R–PDSO–G6) PLASTIC SMALL–OUTLINE PACKAGE



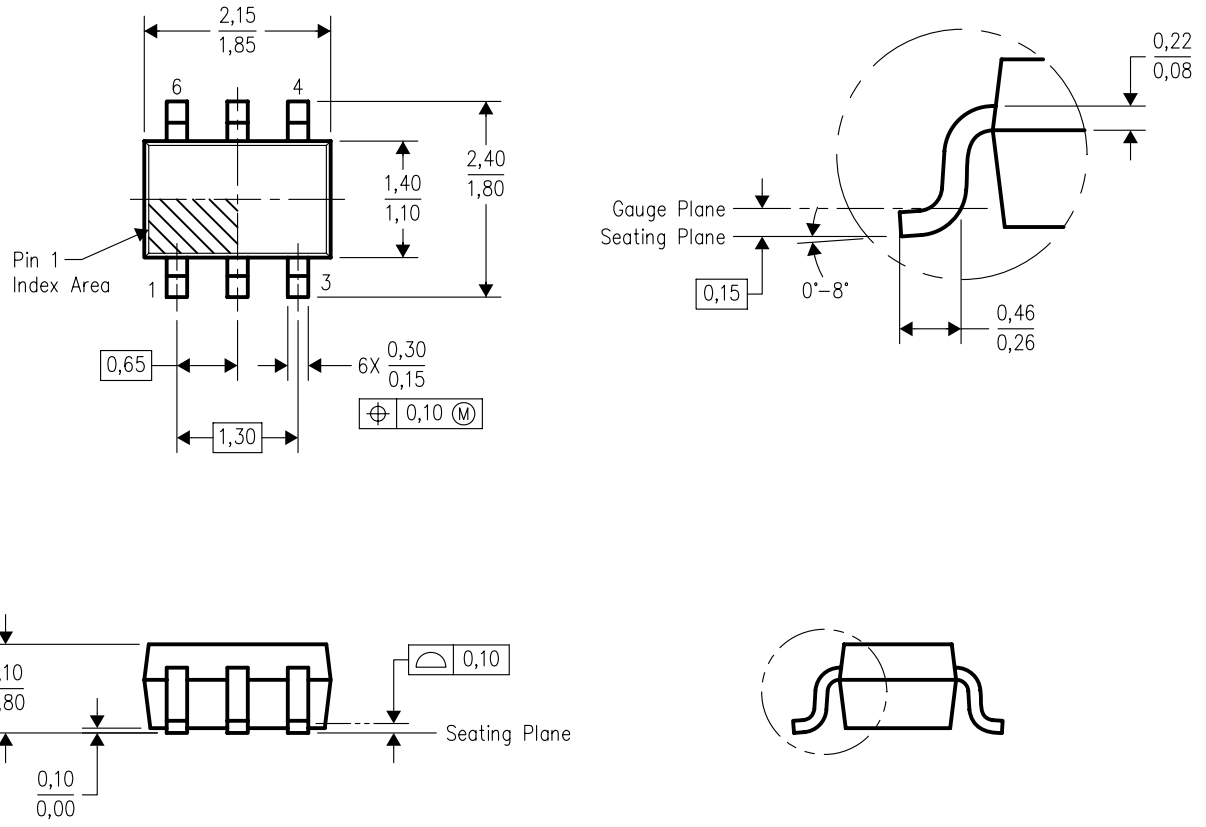
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
E. Falls within JEDEC MO–178 Variation AB, except minimum lead width.

DBV (R–PDSO–G6) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

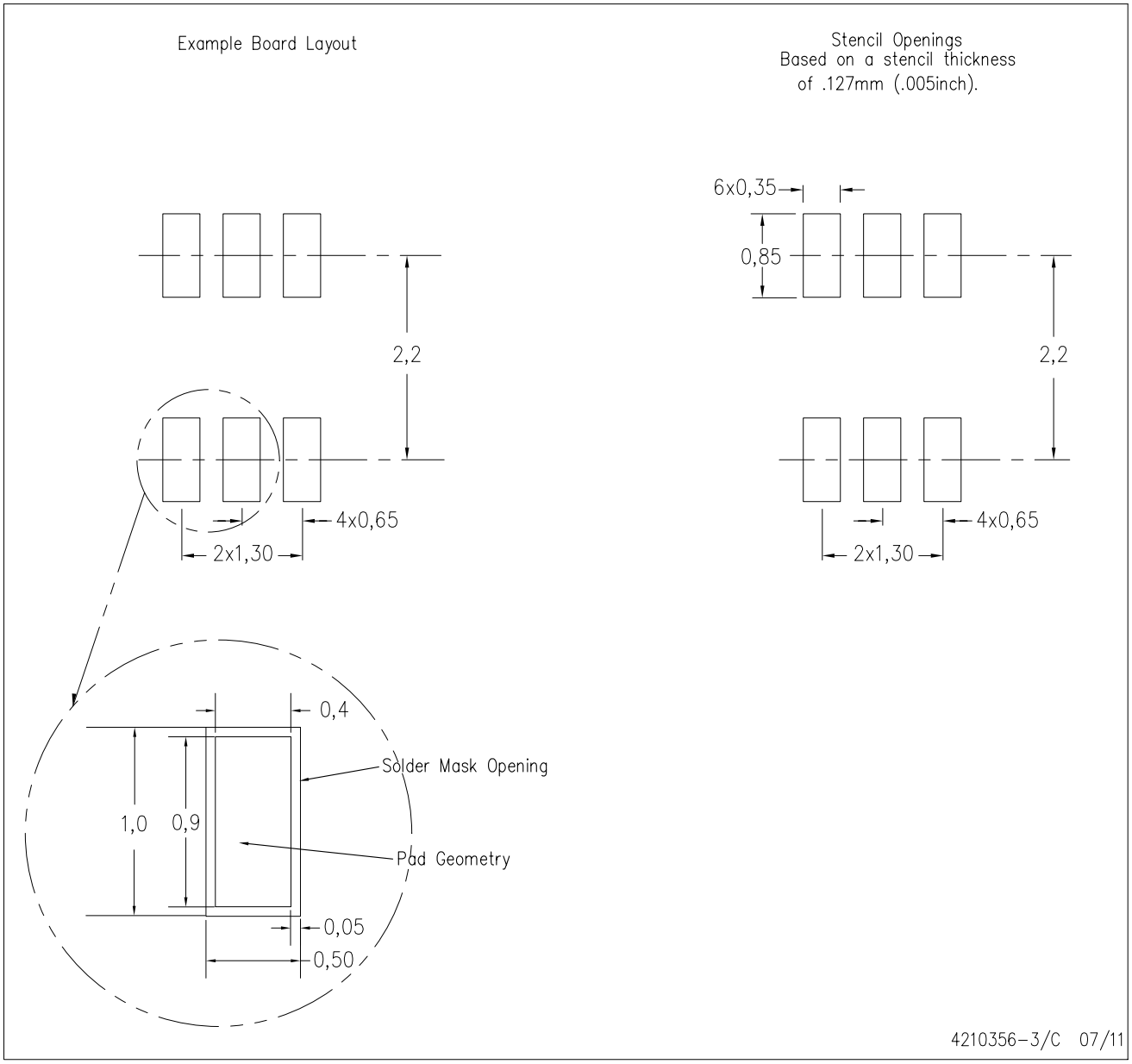
DCK (R–PDSO–G6) PLASTIC SMALL–OUTLINE PACKAGE



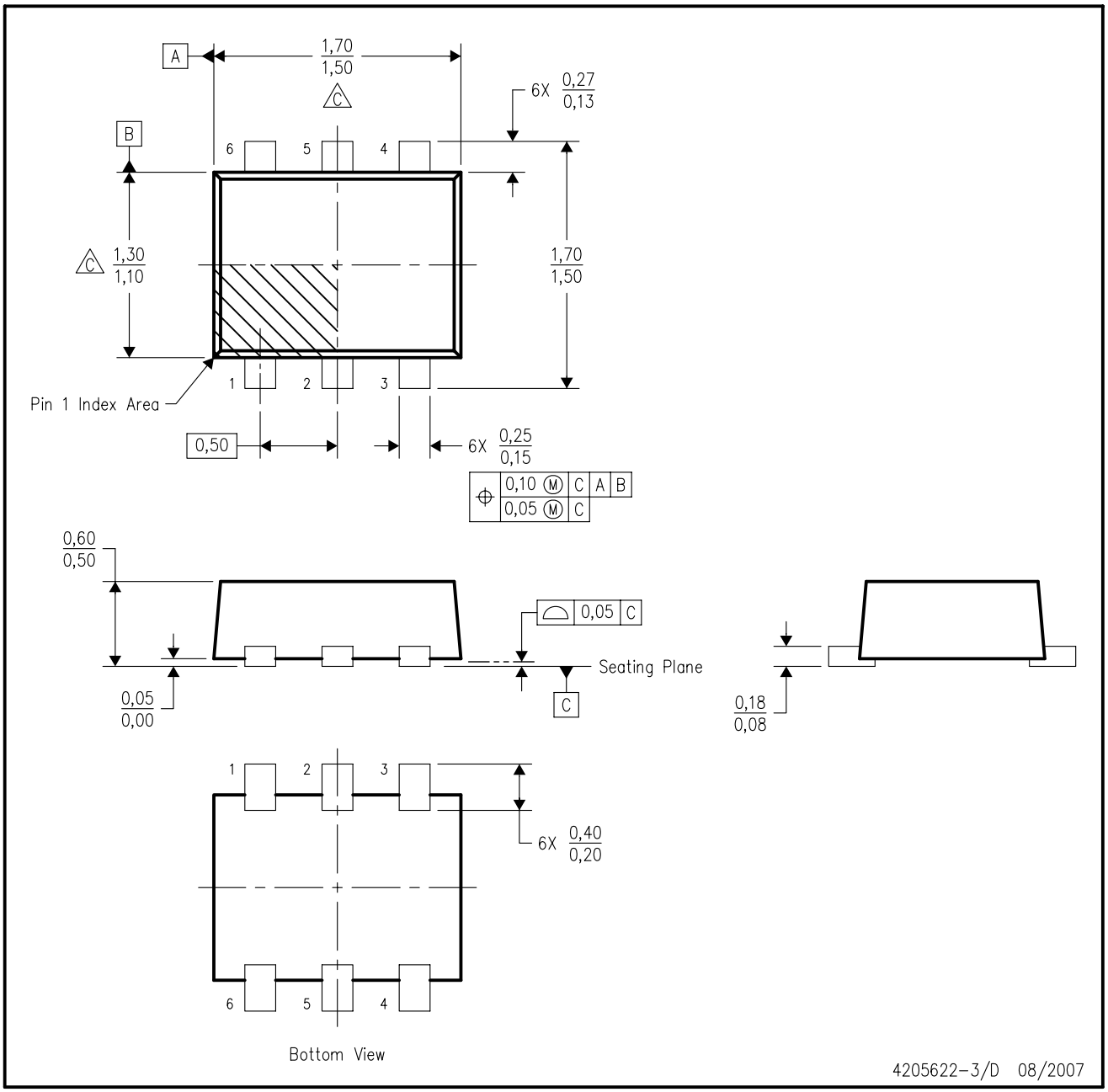
4093553–4/G 01/2007

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AB.

DCK (R–PDSO–G6) PLASTIC SMALL OUTLINE

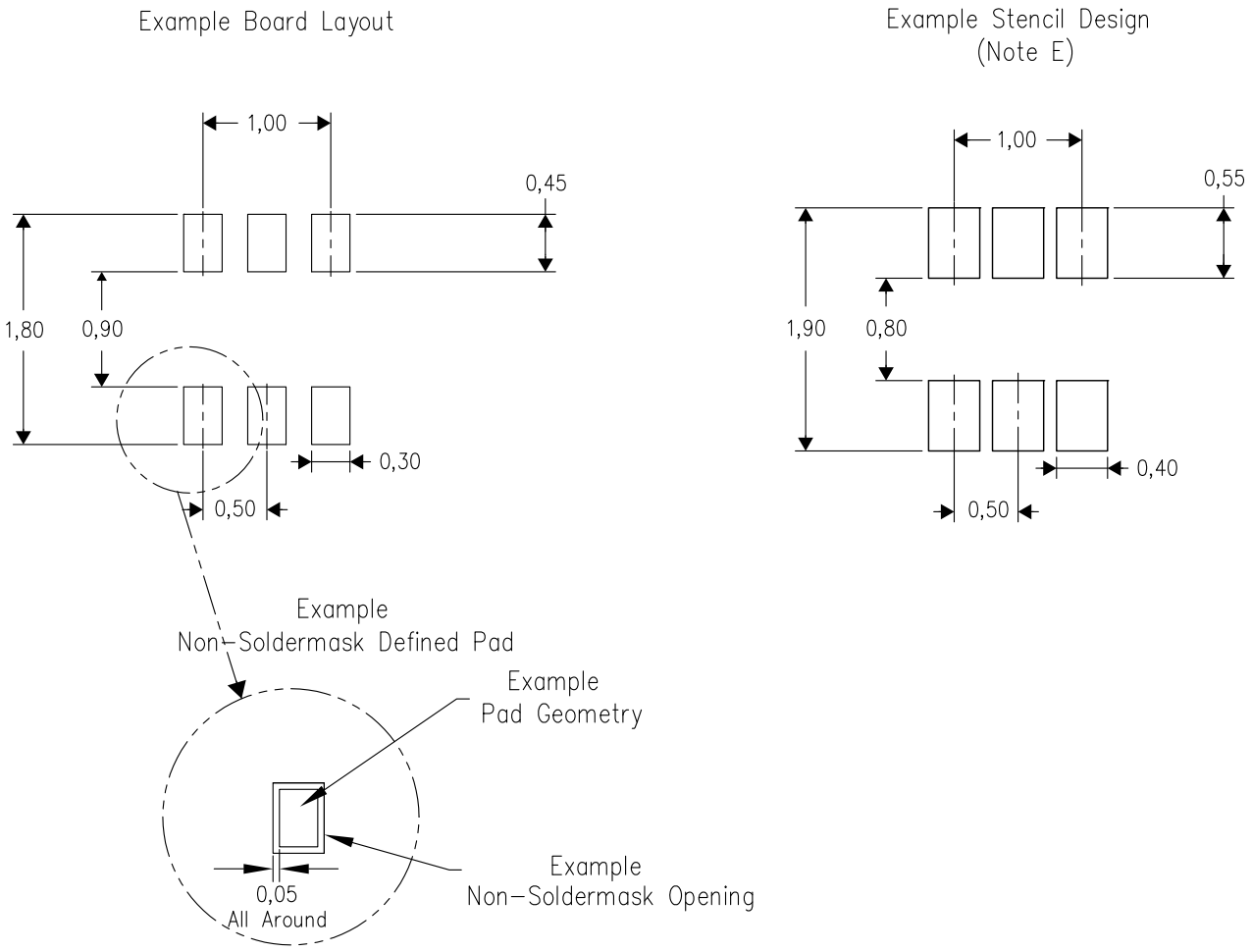


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash, interlead flash, protrusions, or gate burrs. Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0,15 per end or side.
D. JEDEC package registration is pending.

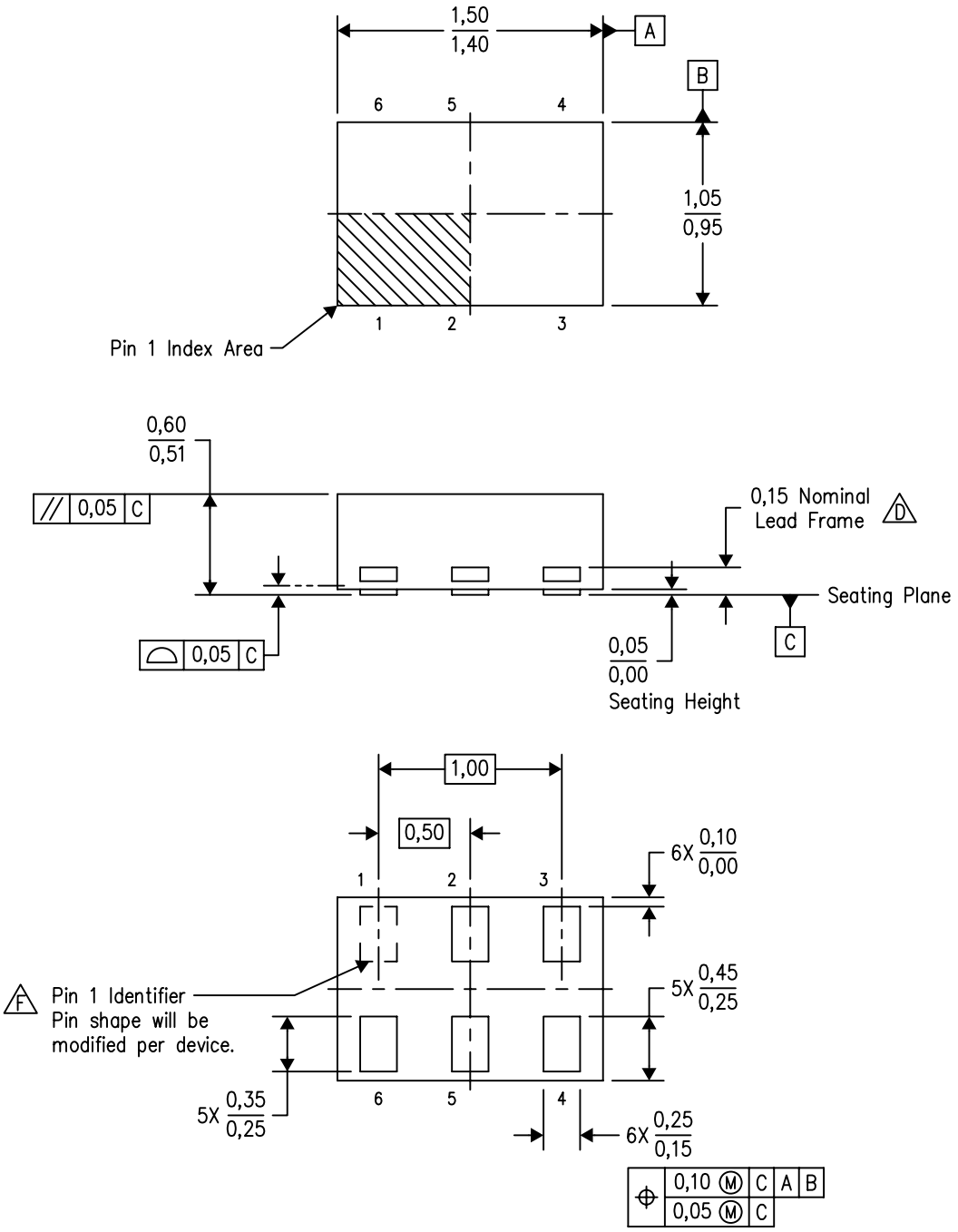
DRL (R–PDSO–N6) PLASTIC SMALL OUTLINE



4208207–3/E 06/12

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

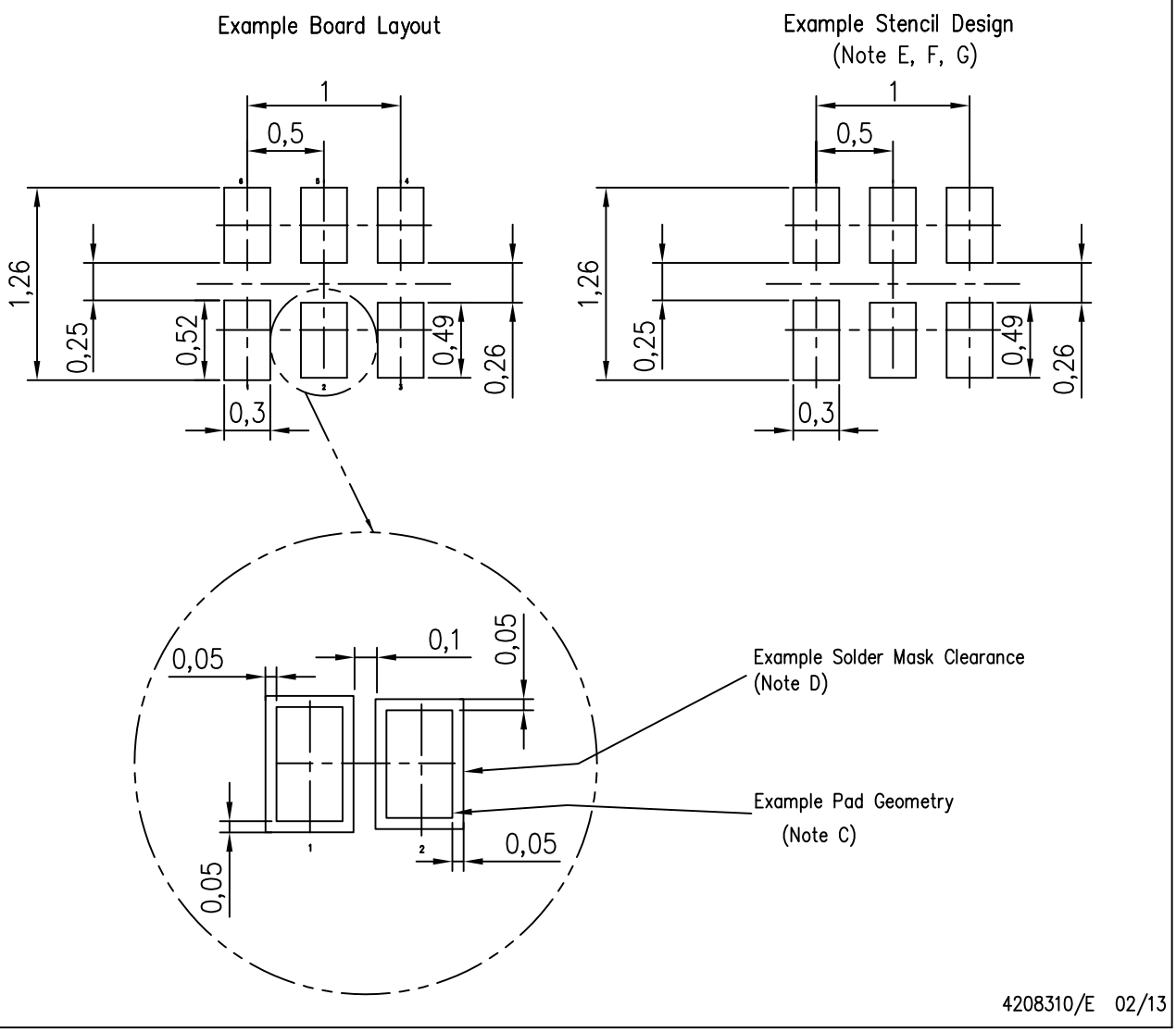
DRY (R–PUSON–N6) PLASTIC SMALL OUTLINE NO–LEAD



4207181/F 12/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.
D. The exposed lead frame feature on side of package may or may not be present due to alternative lead frame designs.
E. This package complies to JEDEC MO–287 variation UFAD.
F. See the additional figure in the Product Data Sheet for details regarding the pin 1 identifier shape.

DRY (R–PUSON–N6) PLASTIC SMALL OUTLINE NO–LEAD



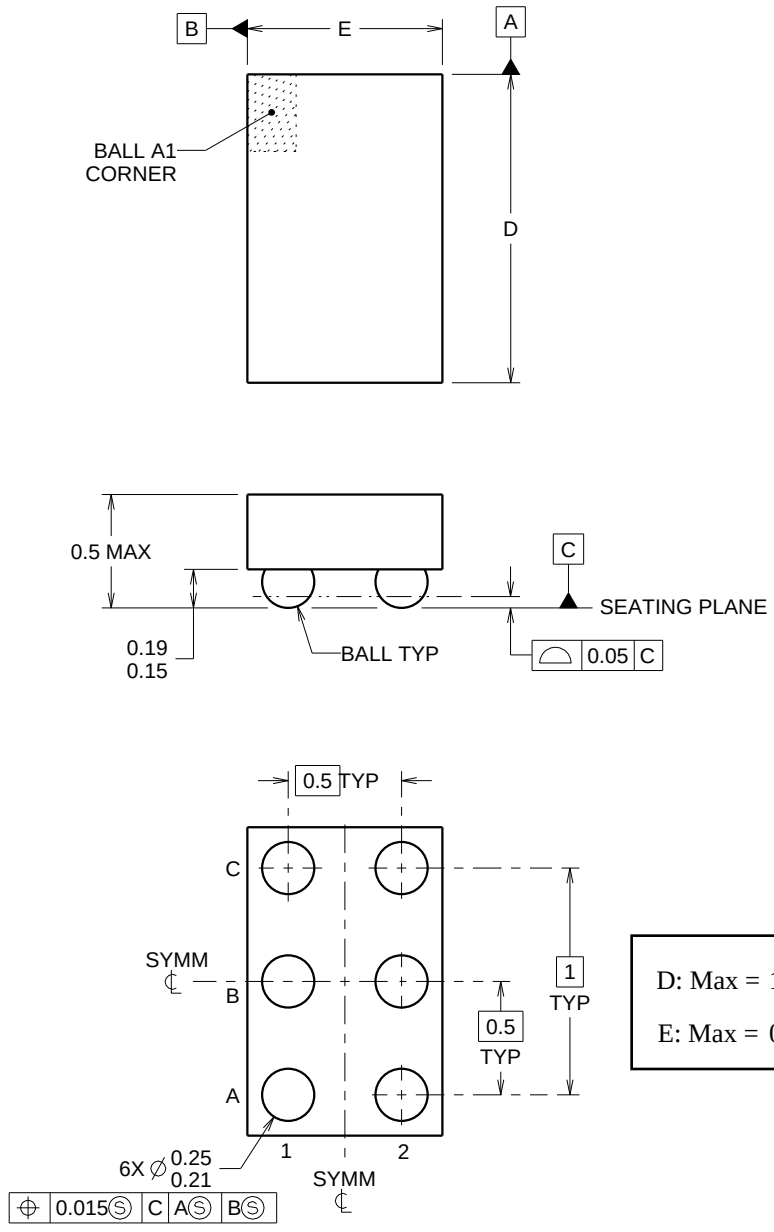
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

PACKAGE OUTLINE

YZP0006

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



D: Max = 1.418 mm, Min =1.357 mm

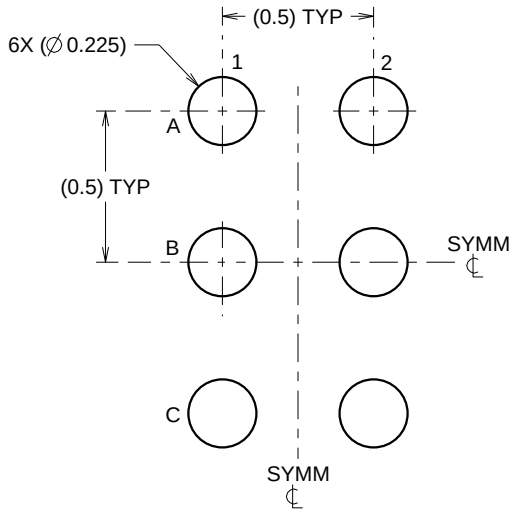
E: Max = 0.918 mm, Min =0.857 mm

4219524/A 06/2014

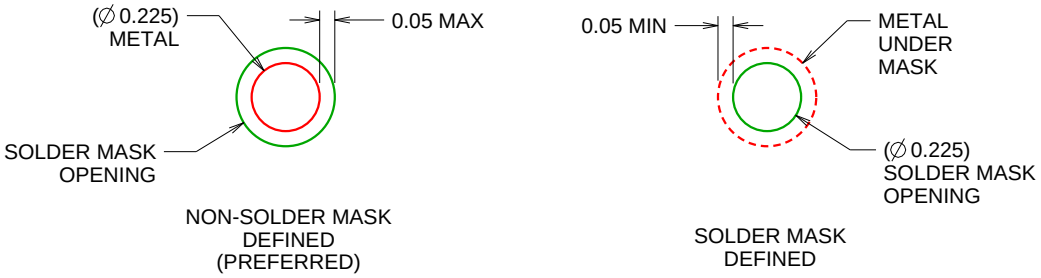
NOTES:

NanoFree Is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. NanoFree™ package configuration.



LAND PATTERN EXAMPLE
SCALE:40X

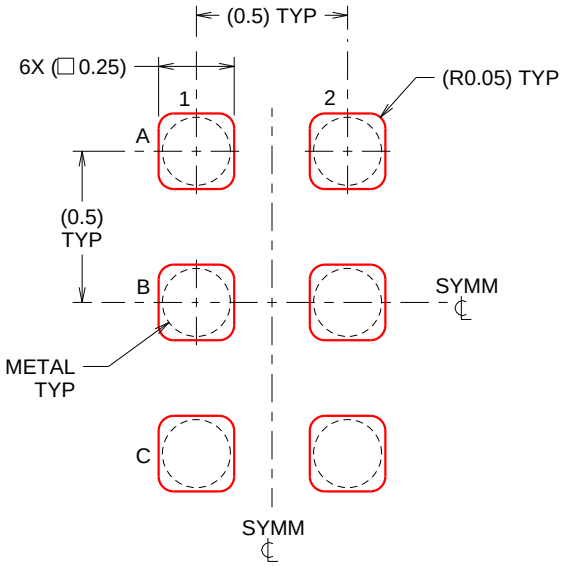


SOLDER MASK DETAILS
NOT TO SCALE

4219524/A 06/2014

NOTES: (continued)

4. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SBVA017 (www.ti.com/lit/sbva017).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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